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Code No: A7008

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech I Semester Examinations, October/November-2011
VHDL MODELING OF DIGITAL SYSTEMS
(ELECTRONICS AND COMMUNICATION ENGINEERING)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks

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1.a) With the help of a block diagram and flow chart, explain about categories of synthesis tools in a design process.
b) Draw the flow chart and explain how verification is done at each design stage. [12]

2.a) Give an example for hierarchical partitioning and explain the same.
b) Explain about the salient features of VHDL with examples. [12]

3. Explain about the following pertaining to VHDL
a) Objects and classes
b) Signals and variables
c) Concurrent and sequential assignments. [12]

4.a) It is desired to remove pulses that are smaller than a certain width. Using any signal assignments write a code fragment for removing positive pulses that are grater than a certain width.
b) Explain about concurrency. [12]

5.a) Write a VHDL description for a package of four NAND gates using signal delay models for each of the gates.
b) Write a VHDL description for a Master-Slave JK-Flip-Flop. [12]

6.a) Write a description for a full adder using 2-input NAND and X-OR gates, in VHDL.
b) Design an 8-bit odd parity checker using X-OR gate. Write a test bench for testing all the input combinations of this circuit. [12]

7. Write a VHDL description for a 3-to-8 decoder, with an active low enable input and an active high enable input. When disabled, all outputs have to be 0. [12]

8. Write notes on any TWO
a) Process statements and assertion statements in VHDL
b) MSI.8 based design
c) Wiring Interactive Networks. [6×2=12]

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